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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/256,643	02/23/1999	LEONARD FORBES	303.324US2	1086

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EXAMINER	
TRINH, MICHAEL MANH	

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2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/256,643	Applicant(s) FORBES ET AL.	
	Examiner Michael M Trinh	Art Unit 2822	

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23,24,26,29-33 and 36-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23,24,26,29-32,36-46,48-61,63-66,68,69 and 71-74* is/are rejected.

7)☒ Claim(s) *33,47,62,67,70 and 75* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *31* .
4) ☒ Interview Summary (PTO-413) Paper No(s). *30* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's response filed on November 18, 2002. Claims 21,23-24,26,29-33,36-75 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102/103

1. Claims 21,23-24,26,29-32,36-46,48-59 are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ohba et al (5,734,181).

Ohba teaches a method for forming a transistor (Figs 2A-2C; col 6, line 4 through col 7) comprising: forming a source region and a drain region in a semiconductor substrate, a channel region being between the source and the drain region, wherein a channel region is formed between the source and drain regions; forming an insulating layer on the channel region; forming a layer of silicon carbide compound $Si_{1-x}C_x$ for forming a gate on the gate insulating layer SiC layer on the insulating layer wherein x of 4/7 is at a value approximately between 0 and 1, since carbon ions implanted into the semiconductor substrate for forming source and drain region 8a,8b are also inherently implanted into the polysilicon gate 6 (col 6, lines 10-15), wherein the method comprising removing portions of the insulating layer to form gate insulating layer 4 and the layer of gate material by patterning and etching to form a gate 6 on the substrate (Figs 2A-2C; col 6, lines 4-5-15, wherein the selected value x of 4/7 inherently yield the claimed barrier energy and charge retention time.

Regarding other limitations including deposition techniques, for example, in claim 40, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation, for example, in claim 42, would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting dopant of p-type or n-type into the gate would have

been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate and to form n-channel device or p-channel device.

Claim Rejections - 35 USC § 103

2. Claims 21,23-24,26,29-32,36-46,48-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamberlain (4,473,836) taken with Halvis et al (5,369,040).

Chamberlain teaches a method for forming a transistor (Figs 2,4; columns 3-6 comprising: forming diffused regions D1,D2 that respectively function as a source region and drain region in a semiconductor silicon substrate (col 3, lines 11-27), wherein a channel region being between the source and drain regions; forming an insulating layer 13 on the channel region; forming a layer of polysilicon material; and patterning and etching to remove portions of the insulating layer and the layer of polysilicon material 14 to form a gate on the substrate.

Chamberlain lacks to form the gate of silicon carbide compound.

However, *Halvis* et al teach (cols 1-2; specifically, col 1, lines 23-30,62-68; col 2, lines 18-30 and 6-15) that it is known to use polysilicon material for forming a gate, and teach (at col 4, lines 10-15; cols 3-4) to use silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5, for forming a gate on the gate insulating layer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Chamberlain with the gate of silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5 as taught by Halvis et al. This is because polysilicon and silicon carbide are art recognized alternative semiconductor materials for substitution in forming the gate, wherein polysilicon and silicon carbide are high electrical conductive materials that is good for forming the gate.

3. Claims 21,23-24,26,29-32,36-46,48-59,60-61,63-66,68-69,71-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al (5,449,941) taken with Halvis et al (5,369,040).

Yamazaki et al teaches a method for forming a MOS transistor for memory cell (Figs 1A-1D; 2A-2D; col 4, lines 12-15; lines 27-60; col 3,lines 66-68) comprising: forming a source region and drain region in a semiconductor silicon substrate 201 (Fig 2A; col 3, lines 35-68),

wherein a channel region being between the source and drain regions 203,204; forming an insulating layer 206/207 on the channel region; forming a floating gate 208 by patterning and etching a layer of gate material; forming an intergate dielectric layer 209; and forming a control gate 210 over the floating gate 208.

Yamazaki lack to form the floating gate of silicon carbide compound.

However, *Halvis* et al teach (at col 4, lines 10-15; cols 3-4), rather using polysilicon gate, using silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5. for forming a gate on the gate insulating layer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5 as taught by Halvis et al. This is because polysilicon and silicon carbide are art recognized alternative semiconductor materials for substitution in forming the gate as combinatively taught by Yamazaki and Halvis et al, wherein polysilicon and silicon carbide are high electrical conductive materials that is good for forming the gate.

Regarding other limitations including deposition techniques, for example, in claim 40, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting dopant into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller*

104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

4. Claims 21,23-24,26,29-32,36-46,48-59,60-61,63-66,68-69,71-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halvis et al (5,369,040) taken with Chamberlain (4,473,836) or Frye et al (4,118,795), and further of Tohyama (5,858,811).

Halvis et al teaches a method for forming a semiconductor device (Figs 4A-4C; cols 3-4) comprising: forming an insulating layer 32 on the channel region; forming a floating gate 38 by patterning and etching a layer of gate material 33 (figs 4A-4B; col 3, line 61 through col 4); forming an intergate dielectric layer 42 by oxidizing; and forming a control gate 50 over the floating gate 38 with the intergate dielectric layers 42 therebetween (Fig 4C).

Halvis lacks to show source and drain regions in the substrate (e.g. claim 21), and further lacks to remove portion of insulating layer during forming of gate 38 (e.g. claims 43,50,etc.).

However, Chamberlain teaches (at col 3, lines 20-27) a photodetector as of Halvis, wherein diffused regions functioned as source and drain regions are formed in the semiconductor substrate that separated by a channel region in the substrate. Frye et al also teach (at Figs 1a ,2a,3a; cols 1-4; col 3, lines 1-10) to form a charge couple device (CCD) comprising gates formed on a gate insulating layer formed on a semiconductor substrate, wherein source and drain regions are formed in the substrate that are separated by a channel region in the substrate. *Tohyama* et al teach (at Fig 1 to 4; col 1-3, cols 5-6) it is alternative either removing portions of the first insulating layer 4 (Fig 3C; col 2, lines 40-63) and the layer of gate material 6 to form a gate 8, or not removing a portion of the first insulating layer 4 (Figs 1C-1D); forming an interlayer dielectric layer; and forming a second gate 13, wherein the gate layer is doped with n-type or p-type impurities (col 6, lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form diffused regions functioned as source and drain regions in the semiconductor substrate that separated by a channel region in the substrate is taught by Chamberlain and Frye et al, and to remove portions of the insulating layer and the layer of silicon carbide of Halvis in forming the gate as taught by Tohyama. This is because of the desirability to use source and drain regions for storing and transferring electrical charge. This is because of the desirability to

control the desired thickness of the gate insulating layer, wherein thickness of each of the gate insulating layers are formed independently from each other.

Regarding other limitations including deposition techniques, for example, in claim 44, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting n-type or p-type dopants into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

Allowable Subject Matter

5. Claims 33,47,62,67,70,75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

*** Applicant's remarks filed November 18, 2002 have been fully considered but they are not persuasive and to be in moot of new ground of rejection.

*** Applicant appears to remark (at 11/18/02 remark pages 1-4) that it would not motivate since Chamberlain states (at col 3, lines 23-26) "...gate G1 includes... aluminum or

polysilicon 14. If polysilicon is employed, it must be covered to be impervious to light, since polysilicon is transparent...", and since the silicon carbide of Halvis is transparent.

In response, it is noted and found unconvincing, since Chamberlain teaches to simply cover the gate if the gate is transparent material. Accordingly, by alternatively using polysilicon or silicon carbide as a gate material, together with a cover layer thereon, the principle of operation of the device of Chamberlain is still the same and would be satisfactory for its intended purpose of detecting incident light. Indeed, as can be seen, Chamberlain teaches the substitution of alternative materials including aluminum or polysilicon even though polysilicon is a transparent material.

Thus, since *Halvis* prima facie teaches (at col 4, lines 10-15; cols 3-4) to use silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5 for forming a gate on the gate insulating layer, instead of using polysilicon gate (cols 1-2; specifically, col 1, lines 23-30,62-68; col 2, lines 18-30 and 6-15), one of ordinary skill in the art would motivate and recognize the alternative use of aluminum, polysilicon or silicon carbide for forming a gate of Chamberlain, if polysilicon or silicon carbide is employed, they must be covered to be impervious to light, since polysilicon or silicon carbide are transparent.

The Examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971): In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

** Applicant further remarks (at remark filed 11/18/02, page 5) that "...the region of D1 in Chamberlain must be exposed to light...", while either Halvis or Tohyama teaches to cover the source and drain regions with an insulating layer that would distort incoming light.

In response, it is noted and found unconvincing. Applicant appears to misinterpret the invention of Chamberlain. The structure as shown in Figure 4 of Chamberlain is not a final

product since other final passivation and protective insulating layer would be formed over the source and drain regions but not shown in the drawing figure. Not shielding region D1 from light is different from forming a protective insulating layer to protect the source and drain regions. Moreover, Frye also teaches to form source and drain regions in the substrate.

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*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner